

## [54] TEST PATTERN ADDRESS GENERATOR

[75] Inventor: Robert D. Catiller, Garden Grove,  
Calif.

[73] Assignee: **Burroughs Corporation, Detroit, Mich.**

[21] Appl. No.: 267,041

[22] Filed: May 26, 1981

[51] Int. Cl.<sup>3</sup> ..... G06F 11/22

[52] U.S. Cl. .... 371/21

[58] **Field of Search** ..... 371/21; 324/73 R

[56] **References Cited**

## U.S. PATENT DOCUMENTS

4,195,770	4/1980	Benton et al. ....	371/21
4,204,633	5/1980	Goel .....	324/73
4,263,669	4/1981	Staiger .....	371/21
4,271,512	6/1981	Lylus .....	371/21
4,332,028	5/1982	Jocotton et al. ....	371/21

**Primary Examiner—Jerry Smith**

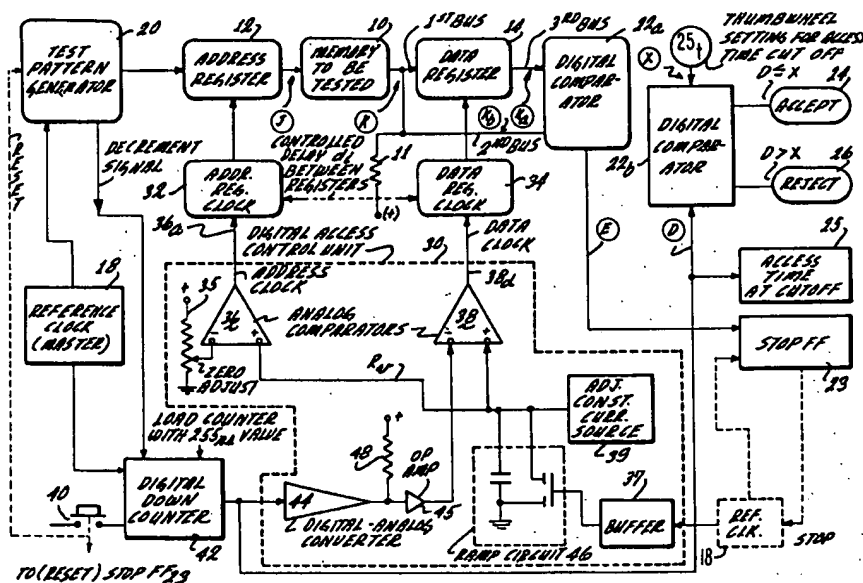
**Assistant Examiner—Michael R. Fleming**

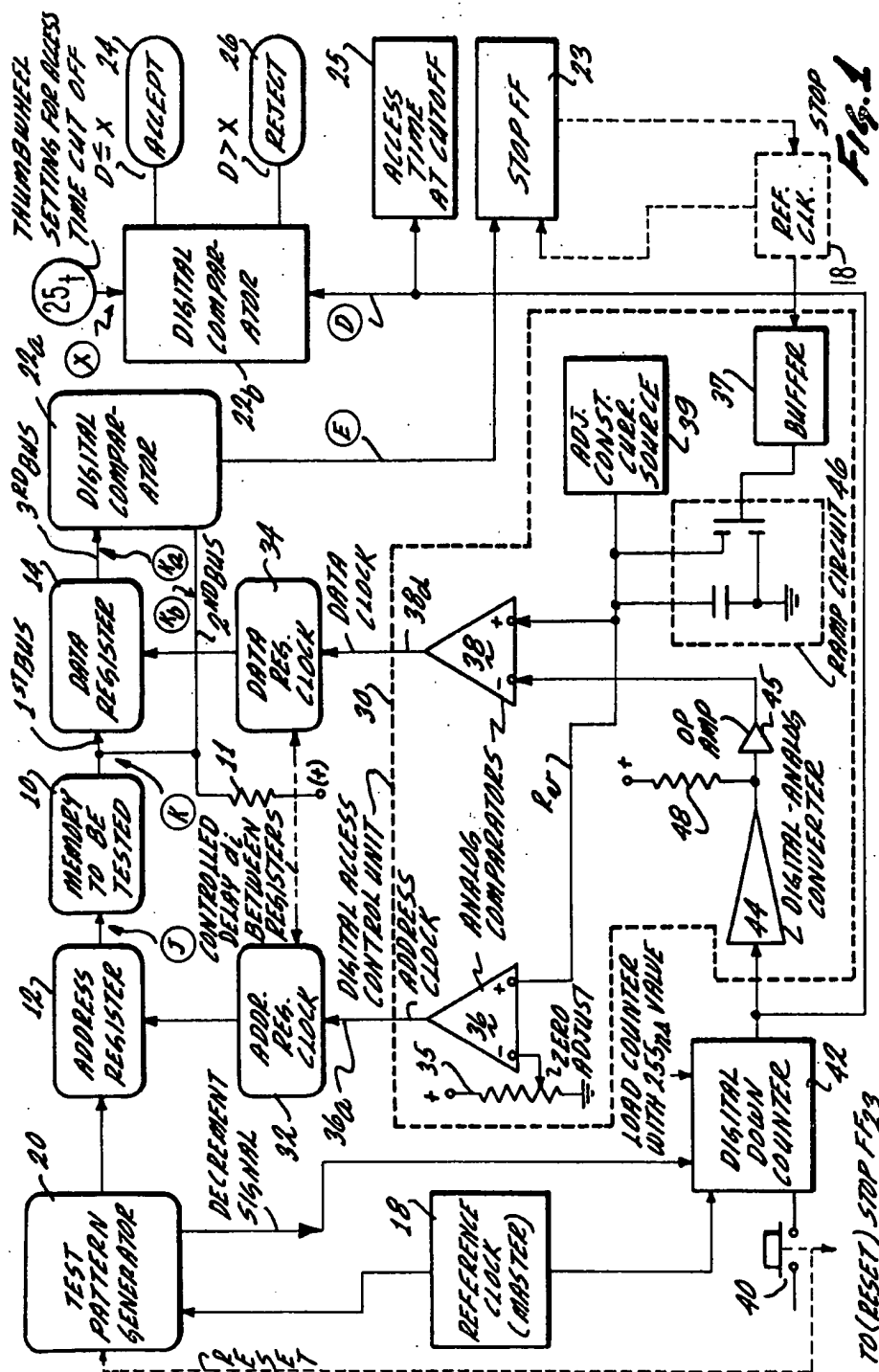
**Attorney, Agent, or Firm**—Alfred W. Kozak; Nathan Cass; Kevin R. Peterson

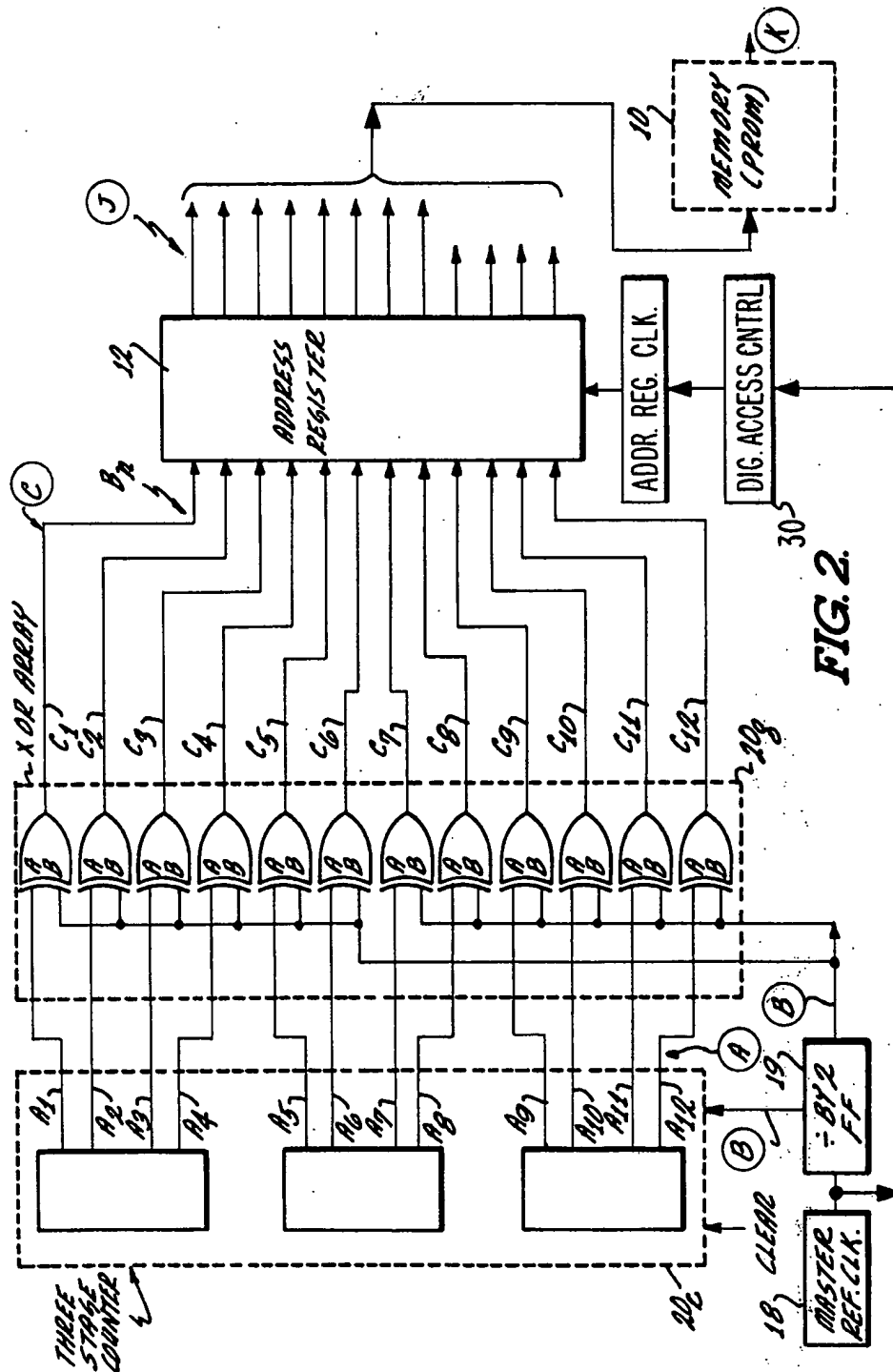
## [57] ABSTRACT

A test pattern generator is used for generating a series of address signals such as for exercising an integrated circuit memory. Master reference clock means are used to trigger a three stage counting circuit and also a circuit array of exclusive OR gates. The outputs of the stages of the counter provide individual inputs to each of the exclusive OR gates. The array of exclusive OR gates is arranged so that each exclusive OR gate has an output line which provides one bit of information for the address signals. The combination of the outputs of the OR gates forms a parallel bus which carries the address signals to be applied to the integrated circuit memory. The circuit generates a specialized address pattern in which the original address generated is complemented, then incremented on a series of increment-complement actions so that all combinations of the row and column drivers in the integrated circuit memory are exercised.

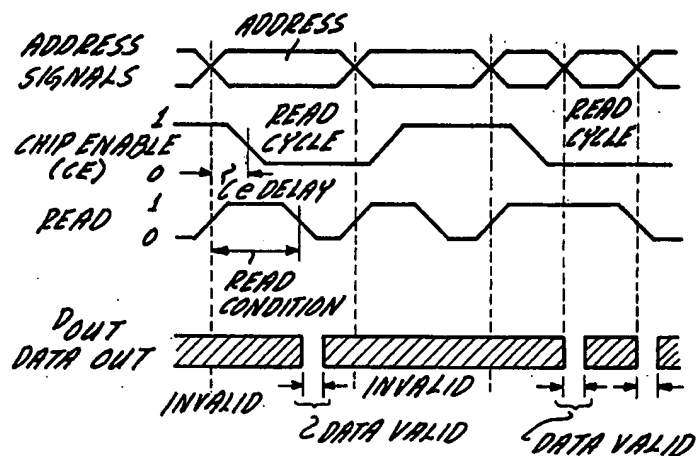
### 11 Claims, 8 Drawing Figures





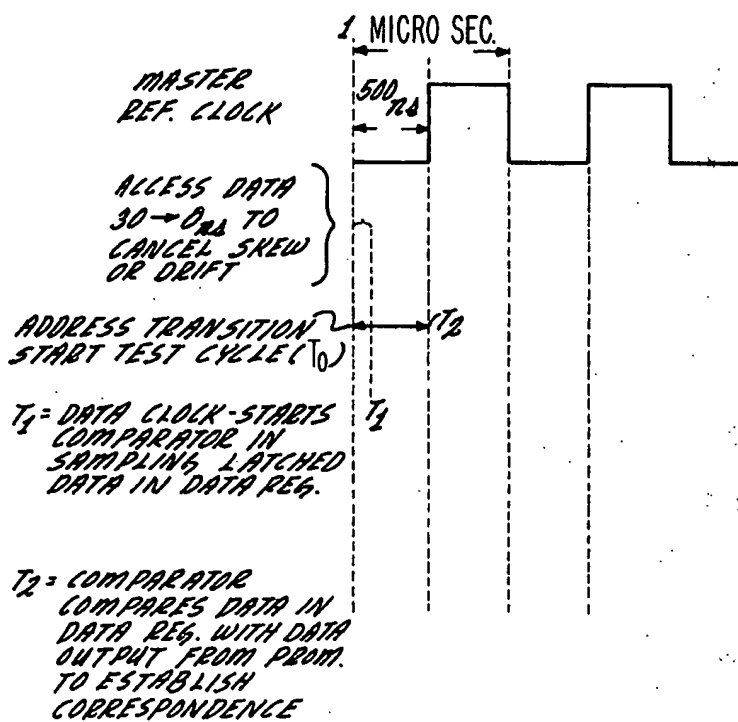




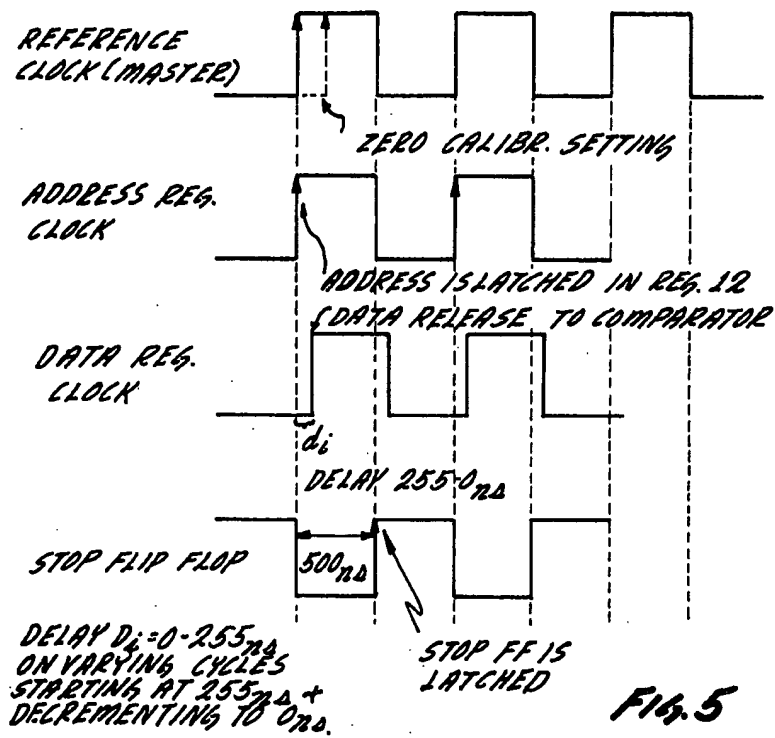
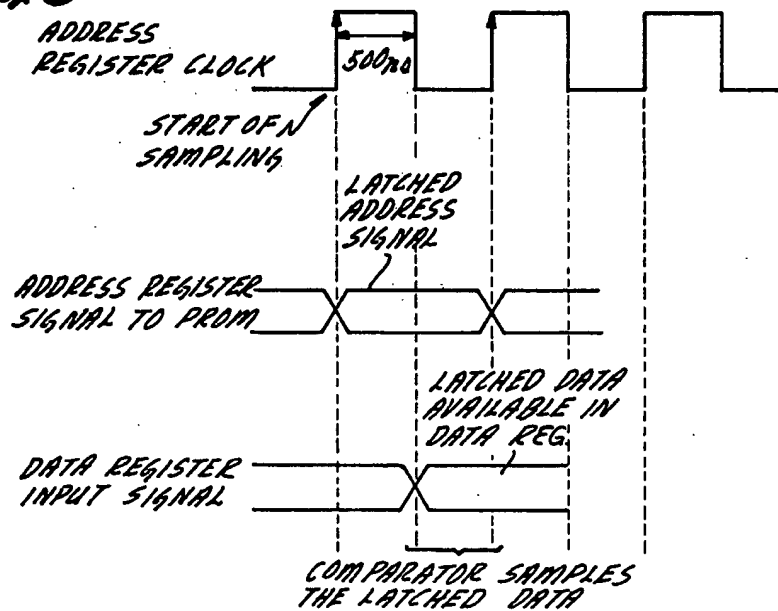


TYPICAL PROM ADDRESS ACCESS CYCLE

**Fig. 4A**



**Fig. 4B**

**Fig. 6**

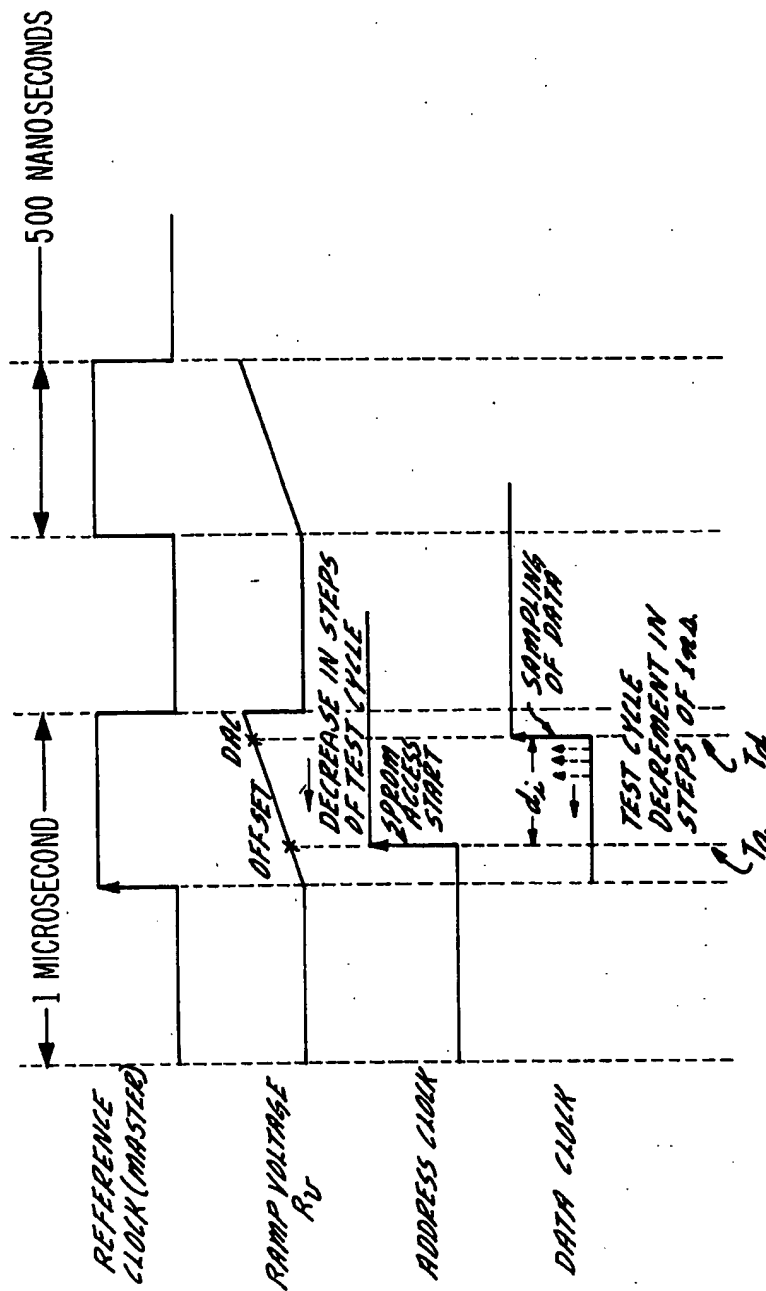


Fig. 7

## TEST PATTERN ADDRESS GENERATOR

### FIELD OF THE INVENTION

This invention relates to the extremely rapid testing of semi-conductor memories such as PROMs and apparatus which facilitates this purpose in an exceptionally inexpensive manner with few components.

### CROSS REFERENCES TO RELATED APPLICATIONS

This application is related to other patent applications filed on the same date and designated as "Comparison Circuit", Ser. No. 267,062, filed May 26, 1981, inventor Robert D. Catiller; a patent application entitled "Dual Clocking Time Delay Generation Circuit", Ser. No. 267,071, filed May 26, 1981, now U.S. Pat. No. 4,379,265 inventor Robert D. Catiller; and also a patent application entitled "Apparatus and Technique for Testing IC Memories", Ser. No. 267,048, filed May 26, 1981, inventor Robert D. Catiller.

### BACKGROUND

With the rapid use of integrated circuit memories and various types of PROM memories, considerable efforts have been made to establish the reliability of such devices and to inspect and test production multitudes of such devices with efforts that are reasonable in time and cost.

In the prior and existing arts, semi-conductor memory devices have been tested with long, expensive and costly procedures whereby a computer is programmed to address all possible data combinations in the tested-memory and then using a previously stored standard of what data should be in the memory, then to make individual comparisons of the standard against each data bits in the tested memory. This required the use of a main computer and main memory, in addition to special programming procedures which were very costly and further required relatively long time periods to exercise the memory and to check all of its internal data with an external standard.

The use of semi-conductor memories and PROMs particularly involves a multi-million dollar industry that is continuously expanding. The use of millions of said semi-conductor memories not only brings up problems of production, but especially of testing that production, to see if the produced items are workable and reliable and especially how quickly the memories can respond (access time) with stable output of accessed data.

Many attempts have been made to handle the problem of weeding out defective PROMs and establishing their access time or speed of response. When defective uncalibrated PROMs get into the production line, they involve systems which can cause untold losses in terms of down time, production loss, customer upset and debugging problems. It is necessary that there be some way of eliminating defective PROMs using minimal testing time in order to save millions of dollars in repairing, debugging and rebuilding systems which might arise from defective or slow PROMs.

Thus, much effort and expense has been devoted to the testing and calibration of the response time of semi-conductor memories. And the expense of such testing can sometimes become almost prohibitive when it requires special programming, special computer appara-

tus, and long periods of operation time in order to test a single memory or a group of memories.

The herein described apparatus and technique for testing of semi-conductor memories involves a very minimal cost of apparatus and provides an automatic test procedure which steps through a series of "access times" of diminishing values (done for each bit accessed from the memory being tested). Upon the first detection of instability or access error, the test cycle is shut off and a display readout is made of the "reliable" time period of access. This permits the tested memory to be identified as to its lowest reliable access time period and below which there is no reliability. The unit described herein can test reliability of memories down to "access time" periods of a few nanoseconds.

### SUMMARY OF THE INVENTION

The present invention involves a pattern address generator for testing Integrated Circuit (IC) memories having row and column drivers. A parallel array of exclusive OR gates are arranged so that the output line of each OR gate provides one address information bit to a bus which simultaneously carries parallel bits of address information. Each OR gate is clocked via a master reference clock which also operates a three stage up-counter. The up-counter provides inputs to each of the exclusive OR gates in the array. The output lines of the OR gates will thus generate a sequential series of addresses which work such that the first provided output address is then complemented in all lines. Then the next sequential address will be the increment of the first or initial address, and then in sequence this particular address will be complemented. Thus, the odd-numbered sequences of address signals will follow a sequential incrementing pattern while the interlaced even numbered sequential address signals generated will constitute the complement of each of the previously established address signals. In this pattern, all the row and column combinations of the IC memory will be exercised.

The present invention resolves the burdensome requirements of long-test-periods, complex programming with a main computer, and need for extensive, complex and expensive apparatus. Now, a relatively few simple elements can be arranged to exercise and test semi-conductor memories with exceptional reliability totally in a period of one second or less and at an equipment and labor cost factor of one-thousandth the cost for prior methods.

A test pattern generator, operating on an increment-complement pattern address system provides a series of addresses which exercise all combinations of the row and column drivers of the semi-conductor memory in a fashion that provides output data resulting from exercising the worst case transitions within the semi-conductor memory. The individual bits of each data word accessed are checked for accuracy during a test period which cycles from 255 nanoseconds down to 0 nanoseconds in order to establish the fastest access time of the output data while still valid and reliable.

The addresses established by the test generator are latched into an address register after which the starting address is clocked into the memory being tested at an initial starting time by means of an address register clock activated from a digital access control unit.

When memory data bits are output from the memory being tested, they are split into two paths. One path of output data is fed directly to a digital comparator while



the other path is latched into a data register. The data latched in the data register is then clocked by a data register clock to the digital comparator which compares the latched data with the directly applied data to ensure that each corresponding bit is equal to its counterpart.

A digital access control unit clocks the address register and then clocks the data register. A controlled delay is established between the data register and the address register for a test cycle which starts at 255 nanoseconds and reduces down to 0 nanoseconds. Thus, for each output data word accessed from the tested memory, the digital comparator makes a series of correspondence tests at the 255 nanosecond level, the 254 nanosecond level, 253 nanosecond level, decrementing 1 nanosecond sequentially in order to make a correspondence test until such time that lack of correspondence of the output data indicates that a point of instability of output has been reached. These lower access time values are thus no longer reliable access periods.

A digital down counter, which cycles from 255 nanoseconds down to 0 nanoseconds for each test period, is connected to energize the digital access control circuit which regulates the delay time between the address clock and the data clock. A second digital comparator provides a thumbwheel adjustable setting for determining the acceptable access time deemed acceptable. A set of displays attached to the second digital comparator will indicate whether a given semi-conductor memory being tested will meet the access time requirements set by the adjustable thumbwheel setting.

One salient feature of the present apparatus and system for PROM testing is that it is not necessary to know the particular data pattern burned into the PROM since the integrity of the data and transitions from one address to a new data address is compared continuously for the previous data access and the later data access. Thus, great savings are possible in the no-longer-needed requirement for storage of the "known" pattern of the PROM which is to be compared to the actual tested pattern of the PROM.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a block diagram of the apparatus for testing semi-conductor memories by establishing the minimum allowable access time for reliable operation.

FIG. 2 is a schematic drawing showing the basic elements of the test pattern generator which generates a sequence of addresses.

FIG. 3 is a schematic drawing of a typical PROM memory being tested by being addressed by the address register and providing output data to a data register.

FIG. 4A shows a timing diagram indicating how the addressing of a typical semi-conductor memory involves delays before output data can be considered as valid data.

FIG. 4B shows a timing diagram illustrating certain parts of the testing cycle.

FIG. 5 is a timing diagram illustrating how a control delay is established between the address register clock and the data register clock.

FIG. 6 is a timing diagram illustrating a time delay between addressing the tested memory and the output of reliable data.

FIG. 7 illustrates the ramp voltage generated by the digital access control module and how this ramp voltage is used to time the address clock and the data clock.

#### GENERAL OPERATION

Referring to FIG. 1, a memory-to-be-tested 10 is connected at points J and K between an address register 12 and data register 14. A test pattern generator 20 generates addresses which exercise the memory 10 by providing a sequence of memory addresses.

The moment of clocking-in the address to the memory 10 is regimented by address clock 32 which starts the test cycle. Subsequently, a predetermined time later, the data clock is triggered from the digital access control unit 30 to convey latched data from data register 14 to a digital comparator 22a. The delay period  $d_i$  between the address clock and the data clock is a variable period which starts at 255 nanoseconds and decrements in steps of 1 nanosecond down toward a 0 delay or 0 nanoseconds of  $d_i$ .

Since the output data of memory 10 appearing at point K is split into two paths, a direct path  $K_b$  and a path which is first latched in data register 14, thus to appear on bus  $K_a$ , the digital comparator 22a can compare the values of the eight bits on bus  $K_a$  with the values of the eight bits of data on bus  $K_b$  at each period of delay  $d_i$  until such time as instability and lack of correspondence occurs between  $K_a$  and  $K_b$ —values which indicate the breakdown point or non-reliability of data at that given "access time".

Thus, when the control delay  $d_i$  is 255 nanoseconds, comparator 22a will compare data of bus  $K_a$  with the data in bus  $K_b$  to see that exact correspondence occurs on the value of each bit. Then the delay  $d_i$  is decremented to 254 nanoseconds and the same comparison between  $K_a$  and  $K_b$  is accomplished. This is again done at 253 nanoseconds, 252 nanoseconds, etc. etc. down to, say for example, 100 nanoseconds, at which time the digital comparator 22a senses that the data on  $K_a$  does not correspond to the data on  $K_b$ . At this moment comparator 22a will trigger the stop flip-flop 23 which will stop the master reference clock 18 and the digital access control unit 30.

A digital down counter 42 is clocked by the master reference clock 18 and loaded with a 255 nanosecond value at the beginning of each test cycle, after which the test pattern generator will provide a decrement signal which recycles the digital down counter so that it decrements its output signal (1 nanosecond at a time) until finally the master clock 18 is turned off (or else a 0 nanosecond period is reached). The digital down counter provides a signal input D to the second digital comparator 22b and also provides an output to an access time display 25. For example, should the stop flip-flop 23 be operated at the 100 nanosecond level (as indicative of non-equality of data on  $K_a$  and  $K_b$ ), then the 100 nanosecond cut-off point would be displayed on the access time display 25.

A second digital comparator 22b has a thumbwheel settable access time cut-off point 25 which provides input to the digital comparator 22b. This is used to set a standard for acceptability or rejectability of a given memory 10 being tested. For example, if the thumbwheel-adjustable setter 25 is set to a period of 50 nanoseconds as the standard cut-off point, then if a memory 10 being tested operates reliably to the point where D is 50 nanoseconds, then the "acceptance display" 24 will operate. If, however, the stop flip-flop shuts off the system before the access time period of 50 nanoseconds is reached, then the digital value D from where D the counter will, of course, be greater than the setting of the

thumbwheel setter (50 nanoseconds) and thus the memory 10 would be considered as a "reject" on display 26.

### DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to FIG. 1 there is seen a memory testing circuit particularly applicable to semi-conductor memories such as bipolar PROMs. A memory to be tested, such as a PROM 10, is connected to an address register 12 and a data register 14 at connection line points J and K. J and K represent bus connections connected to a fixture having connection points whereby the memory 10 can be plugged into the connection points for test purposes and easily removed.

The address register 12 is fed a series of addresses sequentially in a particular test pattern by means of test pattern generator 20 which is clocked by a master reference clock 18 operating under crystal control at a 1 megahertz rate.

Each output address from the test pattern generator 20 is latched into the address register 12 until such time as an address clock signal from address register clock 32 is conveyed to address register 12 to initiate the placement of the address signals on to the memory 10 to be tested.

As seen in FIG. 4A, some period of time occurs after application of the address signals and the "chip enable" signal to provide a read condition, and then eventually the memory 10 outputs a data output signal which becomes "valid" reliable data.

The data output from memory 10, in FIG. 1, is split into two paths at connection point K. Reference to FIG. 3 (showing an 8 bit address system) will show that at connection point K the output lines of the PROM memory 10 being tested are branched into two paths. One path of 8 bit lines is fed to data register 14, while the other branching path of 8 information bit-lines goes directly to the digital comparator 22<sub>a</sub>. The PROM 10 being tested thus provides, at connection point K, output lines to data register 14 which momentarily latches the data and then, upon activation of the data register clock signal 34, places said data bits on the output lines designated K<sub>a</sub> for use of the digital comparator 22<sub>a</sub>. The other path, via direct output line from the PROM 10 to the digital comparator 22<sub>a</sub>, is designated as K<sub>b</sub>.

As seen in FIG. 4B, the address transition to the PROM starts the test cycle. This is at time T<sub>0</sub>. Also there is provided a period of time which is regulatable from 30 nanoseconds to 0 nanoseconds in order to cancel skew, drift or temperature errors, etc., via potentiometer 35, FIG. 1.

At the end of this adjustment period, there occurs a point in time T<sub>1</sub> where the data clock clocks the data in the data register 14 so that it may be sampled by the comparator 22<sub>a</sub>. Then, during the period from T<sub>1</sub> over to T<sub>2</sub>, the comparator 22<sub>a</sub> compares the data which had been latched in the data register with the data being directly output from the PROM in order to check that each bit of each word is in exact equal correspondence. This establishes the "valid" or acceptable output condition of the PROM.

The address register 12 is clocked by an address register clock 32 at the time T<sub>0</sub> shown in FIG. 4B. The data register 14 is clocked by a data register clock 34 of FIG. 1 which time point is shown as T<sub>1</sub> in FIG. 4B. It is at this point that the digital comparator 22<sub>a</sub> will sample the latched data in data register 14 in order to compare it with the direct data received on bus K<sub>b</sub>. This sampling

and comparison of data by the digital comparator 22<sub>a</sub> continues to occur until time T<sub>2</sub> which represents 500 nanoseconds or one-half clock cycle of the master reference clock 18.

It will be seen that there is a time delay between the positive transition of the address clock 32 and the positive transition of the data register clock 34 as will be seen in FIG. 5 and marked as the delay d<sub>i</sub>. This delay period d<sub>i</sub> between the address register clock 32 and the data register clock 34 is a period of time which continuously varies, starting at 255 nanoseconds and decrementing in units of 1 nanosecond and continues decrementing until such time as the stop flip-flop 23 of FIG. 1 is shut off by a signal from the digital comparator 22<sub>a</sub> which signifies that the comparison of bits between bus K<sub>a</sub> and bus K<sub>b</sub> is no longer validly correspondent.

The address clock line 36<sub>a</sub> of FIG. 1 and the data clock line 38<sub>a</sub>, having between them a predetermined delay time d<sub>i</sub>, are provided as outputs from a digital access control unit 30 shown in FIG. 1. The delay d<sub>i</sub> constitutes a test cycle period whereby the delay d<sub>i</sub> is a sequential set of cycles whereby at each individual delay period (255 nanoseconds, 254 nanoseconds, 253 nanoseconds, —100 nanoseconds, 99 nanoseconds, 98 nanoseconds, —down to 1 nanosecond)—each of these individual delay periods is used to provide a complete address exercise of the memory 10 and a consequent checkout for output of valid data as between K<sub>a</sub> and K<sub>b</sub>. Should the digital comparator 22<sub>a</sub>, while testing a particular delay period d<sub>i</sub>, find that the corresponding bits of bus K<sub>a</sub> and bus K<sub>b</sub> are no longer equal in value (that is, in validity and certainty), then the digital comparator 22<sub>a</sub> will send a signal to stop flip-flop 23 to shut off the master reference clock 18 which then shuts off the digital down counter 42 and the digital access control unit 30.

Thus, the testing of the memory 10 is done on an "automatic" basis in that memory 10 is plugged into the fixture at J and K, then the push button 40 is depressed to load the digital down counter 42 with a 255 nanosecond value for cycling purposes. This 255 nanosecond value is decremented by a signal from the test pattern generator 20 such that the counter 42 will decrement in steps of 1 nanosecond downward toward 0 nanoseconds. The test cycle from 255 nanoseconds down to 0 nanoseconds would fully occur should the memory 10 be perfect and have a 0 nanosecond access time whereby digital comparator 22<sub>a</sub> would not have sent a signal to stop flip-flop 23 to shut down the test cycle. Normally there would be a time period, be it 100 nanoseconds, 50 nanoseconds, 30 nanoseconds, etc., whereby the comparison between buses K<sub>a</sub> and K<sub>b</sub> will become uncertain and invalid, thus causing the stop flip-flop to be activated to shut down the master reference clock 18 and the down counter 42 and the digital access control unit 30.

### DIGITAL ACCESS CONTROL UNIT

Referring to FIG. 7, it will be seen that during the rising half-cycle of said master clock 18, there is generated a ramp voltage R<sub>v</sub> having a positive increasing slope. This voltage is generated on line R<sub>v</sub> of FIG. 1 by the action of the adjustable constant current source 39 and ramp circuit 46 which consists of a bank of capacitors. Circuit 46 is energized by master clock signals 18 via buffer 37.

Analog comparator 36 in FIG. 1 receives a voltage on its minus terminal from zero-adjust potentiometer 35.

The plus terminal of analog comparator 36 receives the rising ramp voltage (FIG. 7). When the voltages on the plus and minus terminals are equal, the "offset point" on FIG. 7 establishes the start (rise pulse) of the address clock.

Analog comparator 38 has its positive terminal linked to the ramp voltage  $R$ , while its negative terminal receives a voltage representative of the test-time period being output by the down counter 42.

When the analog voltage from the down counter 42 is equal to the ramp voltage  $R$ , then the DAC (digital access control) point on FIG. 7 is established. At this point in time, the analog comparator 38 puts out the data clock signal which clocks the data register 14 to enable sampling by digital comparator 22<sub>a</sub> on line  $K_a$ .

In FIG. 7, the delay period,  $d_i$ , is seen as that time between the address clock and the data clock rise-pulse signals. This delay period  $d_i$  will originate at a 255 ns period and decrement in steps of 1 nanosecond down to 0 nanoseconds unless the stop flip-flop 23 terminates the sequence of testing periods.

At each discrete delay ( $d_i$ ) test time period, the memory under test is fully exercised for output data to the comparator 22<sub>a</sub>.

The slope (FIG. 7) of the ramp voltage  $R$ , is adjustable via the adjustable constant current source 39 of FIG. 1.

The "offset" point in FIG. 7 is used to eliminate skew, temperature drift and other variables. This is done by adjustment of potentiometer 35.

The ramp circuit 46 of FIG. 1 provides a positive increase in voltage to the positive terminals of each of the analog comparators 36 and 38. The ramp voltage line  $R$ , shown in FIG. 7 is initiated by the positive transition of the reference master clock 18. Ramp circuit 46 is fed by buffer 37 which is clocked by reference clock 18.

Analog comparator 36 has its negative (or minus) connection to a potentiometer 35 which is used for zero adjust in order to cancel drift and skew. Analog comparator 38 has its negative (or minus) terminal fed from an operational amplifier 45 which is supplied by the digital analog converter 44. Converter 44 is activated by the digital down counter 42 which has digital voltage pulses representative of varying time periods.

Thus, in both cases the ramp voltage (from circuit 46 and source 39) is used as a basis of comparison against in one case the analog representation (on the negative terminal of 38) of the digital down counter 42, and in the other case an analog voltage (on the negative terminal of 36) which has been used to cancel drift and skew, thus setting a base point of reference.

The digital down counter 42 is clocked by the master reference clock 18 and is started by depression of push button 40 at which time the digital down counter 42 is loaded with a 255 nanosecond time output signal. After the memory 10 is fully exercised at the 255 nanosecond delay time level  $d_i$ , it is then decremented by the test pattern generator 20 so as to provide a 254 nanosecond time signal during which the memory 10 is again fully exercised and compared by the digital comparator 22<sub>a</sub>. The digital down counter has an output line which feeds into the digital access control unit 30 and specifically to digital analog converter 44. The output of converter 44 is fed to an operational amplifier 45 providing an output to the negative side of analog comparator 38. The positive input to analog comparator 38 is a ramp voltage  $R$ , which is provided by ramp circuit 46 operat-

ing with the adjustable constant current source 39 and being clocked through buffer 37 from reference clock 18. Analog comparator 38 provides the data clock signal to the data register clock 34 and data register 14.

The analog comparator 36 has its positive input provided through the ramp voltage line  $R$ , while the negative input to comparator 36 is a zero adjust potentiometer 35. The output of digital analog converter 44 is normally held at a positive level through resistor 48.

The analog comparator 36 provides an address clock output line to the address register clock 32.

As will be seen in FIG. 7, the ramp voltage  $R$ , is initiated on the positive transition of the reference master clock. The ramp voltage rises to the "offset" point which has been set by the zero adjust potentiometer 35. It is at this point that the address clock will transition in the positive direction causing the address register 12 to place the address signals on the memory 10.

During the positive transition of the master reference clock, the ramp voltage  $R$ , continues to rise to the point (FIG. 7) labelled DAC at which time comparator 38 will place an output signal to the data register clock 34 which will clock the latched data from data register 14 onto the bus lines  $K_a$  for comparison by the digital comparator 22<sub>a</sub>.

#### TEST PATTERN GENERATOR

In FIG. 2 there is shown a test pattern generator 20 which provides address signals to an address register 12. The address register latches these address signals until such time as there occurs a positive transition of the address register clock 32 which places the address signals onto the memory 10.

The test pattern generator 20 primarily consists of a three stage counter 20<sub>c</sub> having outputs A from each stage which feed to individual Exclusive OR gates in gate unit 20<sub>g</sub>. The second input to each of the Exclusive OR gates, which is designated as input B, is derived from a divide-by-two-flip-flop 19 which is clocked by the master reference clock 18. The output B is also fed to the three stage counter for clocking purposes.

The test pattern generator 20 provides a particular sequential pattern which might be described as an increment-complement output address pattern. This pattern is such that after the initial address is provided to the address register, then the address is complemented to provide the next address. Then the original address, for example 001, is incremented to provide an output address signal of 011. Then the 011 address is complemented to give 100. Now the 011 former address is incremented to give an address of 111. This increment-decrement pattern is shown in the following table below where a, b, c, d, and e show the increment complement transitions.

Thus, the test pattern generator 20 can operate on the pattern of choosing an address and then complementing it, such as:

		Address	Initial address
a	a <sub>1</sub>	Address 001	Initial address
	a <sub>2</sub>	Address 110	Complement of initial address
b	b <sub>1</sub>	Address 011	Increment of a <sub>1</sub>
	b <sub>2</sub>	Address 100	Complement of b <sub>1</sub>
c	c <sub>1</sub>	Address 111	Increment of b <sub>1</sub>
	c <sub>2</sub>	Address 000	Complement of b <sub>1</sub>
d	d <sub>1</sub>	Address 100	Increment of c <sub>1</sub>
	d <sub>2</sub>	Address 011	Complement of c <sub>1</sub>

-continued

c	d <sub>2</sub>	Address 011	Complement of c <sub>1</sub>
	e <sub>1</sub>	Address 110	Increment of d <sub>1</sub>
	e <sub>2</sub>	Address 001	Complement of e <sub>1</sub>

By this means of addressing the PROM memory 10 to be tested, there is exercised all the combinations of the matrix, that is, all the row and column combinations that can be addressed plus the complement (transition) of each address.

This means of generating addresses for the PROM memory test cycles will exercise all the combinations of the matrix, that is all the row and column combinations that can be exercised. This can be done very rapidly or in a matter of time less than 500 nanoseconds so that a complete test cycle of any given access time can be effectuated during one-half clock of the master reference clocking cycle.

This address generation pattern is deemed to be much more effective than the standard types of N<sup>2</sup> test generator pattern which involve complex programming and include multiple redundancy of transitions which take considerable periods of time for accomplishment. The increment-complement address pattern actually makes use of the most effective part of the old N<sup>2</sup> patterns, this being those address changes where the most transitions occur, that is the most active transition areas.

The increment-complement generation system eliminates the redundancies in the N<sup>2</sup> system and further exercises all the rows and columns of the PROM drivers in a fashion whereby addresses are sequenced through the pattern shown in the above cited table, which tests the "worst case" transitions.

The Exclusive OR circuits of FIG. 2 can be looked upon as programmed inverters, which do the action of complementing or not complementing and provide addresses which exercise all the combinations of the rows and the columns, the result being that the test pattern generator provides an exercise of the general worst case situations of any PROM which could be tested.

#### OPERATION OF TEST PATTERN GENERATOR:

With reference to FIG. 2, activation of push button 40 (FIG. 1) will "clear" the counter 20<sub>c</sub> so that all counter output lines A<sub>1</sub>-A<sub>12</sub> are equal to zero (0). This action will also reset the halt or stop flip-flop 23 (FIG. 1). The counter 20<sub>c</sub> is an "up" counter which increases its digital output as it gets clocked.

Activation of push button 40 will also reset digital down counter 42 to all "1"s since this counter 42 is a "down" counter which starts at its high value and counts down to lower values. The initial counter value of counter 42 represents a 255 nanosecond test period.

In FIG. 2 the up counter 20<sub>c</sub> will initially present all "0"s on output lines A<sub>1</sub> through A<sub>12</sub>. These lines are each connected to the "A" input of a separate Exclusive OR gate situated in a parallel gate array unit 20<sub>g</sub>.

The master clock 18 energizes a divide-by-two flip-flop 19. Flip-flop 19 has an output B which clocks the up counter 20<sub>c</sub> and provides a series of clock lines B to each Exclusive OR gate in array 20<sub>g</sub>.

Thus, each of the bit-lines A<sub>1</sub>-A<sub>12</sub> will have their information content appear on output lines C<sub>1</sub>-C<sub>12</sub> in a sequence of address patterns. Thus, the initial address lines A<sub>1</sub>-A<sub>12</sub> will first appear (at C<sub>1</sub>-C<sub>12</sub>) as 0000 0000

0000 before the flip-flop 19 goes into its transition to "1".

When this occurs, the OR gates act as inverters and all the output address lines become 1111 1111 1111. Thus, the initial "zeros" address has been complemented.

At the next clock, the counter 20<sub>c</sub> will have its output address lines (A<sub>1</sub>-A<sub>12</sub>) incremented up by "one" so as to constitute

0000 0000 0001.

Now when the clock signal on line B transitions to "1", then the Exclusive OR gates will invert the address signal at C(C<sub>1</sub>-C<sub>12</sub>), to read

1111 1111 1110

which is the complement of the previous address.

Thus, there is generated a sequence of output addresses which follow this pattern:

a<sub>1</sub>=initial address  
a<sub>2</sub>=complement of a<sub>1</sub>  
a<sub>3</sub>=a<sub>1</sub> incremented by "1"  
a<sub>4</sub>=complement of a<sub>3</sub>  
a<sub>5</sub>=a<sub>3</sub> incremented by "1"  
a<sub>6</sub>=complement of a<sub>5</sub>  
and so on.

Another expression of this sequence could be:

a<sub>1</sub>=a<sub>2</sub>  
a<sub>2</sub>=a<sub>1</sub>  
a<sub>3</sub>=(a<sub>2</sub>+1)  
a<sub>4</sub>=(a<sub>3</sub>+1).

Thus, when flip-flop 19 is "low" (0), there is no inversion of the value of signal lines A and signal lines C. For example here, if the outputs (A<sub>1</sub>-A<sub>12</sub>) from counter 20<sub>c</sub> are all "zeros", then the address lines (C<sub>1</sub>-C<sub>12</sub>) to address register 12 will all be "0" also.

When flip-flop 19 goes "high" (1) at its rising edge, then the B inputs to each Exclusive OR gate will invert the signal at C to be the complement of the input signal at A.

The rising edge (0-1) of the flip-flop 19 increments the counter 20<sub>c</sub> by 1 count.

In FIG. 1, it should be noted that the master clock 18 also operates through buffer 37 to initiate a ramp voltage R, through ramp circuit 46. This ramp voltage will enable a "test-pass period" of 255 nanoseconds (initially). During this "test pass" period, there will occur 2<sup>12</sup> increments to counter 20<sub>c</sub> which will exercise all the row and column combinations of memory 10. This "test-pass period" is next run at 254 ns, 253 ns, 252 ns—until the stop flip-flop 23 shuts off the master clock 18.

It may be indicated that no large units of control logic are required here in that the counters operate as "sequencers" and perform their natural function.

The down counter 42 controls the sequences of test-passes which will reveal the access time of memory-under-test 10 to the point where unreliability occurs. The test pattern generator 20 generates the test-pattern addresses for each test-pass period.

#### DIGITAL COMPARATOR CIRCUITRY

The digital comparator 22 may be of the type, for example, as cited on page 7-64 of the Texas Instruments

Company TTL Data Book, 2nd edition, 1976. The output of this type of digital comparator involves three output signal lines which represent the condition of "greater than", the condition of "equal to", or the condition "less than".

The first digital comparator 22<sub>a</sub> when it detects an uncertainty or inequality of comparison between its two input bus lines will signal a "stop" flip-flop which will turn off the master reference clock and end the cycle of testing activity. Then and only when the "stop flip-flop" 23 has been triggered by an error signal, only then will the digital comparator 22<sub>b</sub> operate to check the standard threshold value (set by the thumbwheel) against the time period it took from the start of a test until non-equality (or activation of the stop flip-flop 23) in order to tell, via an output signal, whether the "time period-to-reach-the-error-point" was greater in value than the standard threshold value, thus displaying the memory as not acceptable.

As seen in FIG. 1, the digital comparator 22<sub>a</sub> receives two input bus lines designated as K<sub>a</sub> and K<sub>b</sub>. As seen in FIG. 3, K<sub>b</sub> and K<sub>a</sub> may consist of eight separate information bit lines. The data on the eight bit-lines of K<sub>a</sub> and K<sub>b</sub> are derived from the same source connection point at K.

The data signals on the eight bit-lines of K<sub>a</sub> come from the data register 14 where they have had a chance to settle down by having been latched for a period in the data register 14. The data on the bit-lines of K<sub>b</sub> come directly from the point K.

At each discrete delay period of d<sub>i</sub> (FIG. 5) the output data from the address memory 10 is checked for equal correspondency. When this equal correspondency occurs, the output data from memory 10 is seen to be valid stable data.

The second digital comparator 22<sub>b</sub> has a digital value input line D which is derived from the digital down counter 42. This presents to the comparator 22<sub>b</sub> a present moment indication of the nanosecond time period being tested for. This value of D is shown on the access time display unit 25 which access time unit will indicate each of the nanosecond time-test periods from 255 nanoseconds on downward in decrements of 1 nanosecond.

Another input to the digital comparator 22<sub>b</sub> is the settable thumbwheel 25 which provides an output signal X which represents the minimum access time for a PROM memory to be considered acceptable. Thus, if a memory 10 being tested shuts off the stop flip-flop 23 before reaching the value of X (D greater than X), then the "reject" display light 26 will light up telling the operator that the PROM 10 is unacceptable. On the other hand if the digital down counter and the digital value D continues to decrement to a value which is lesser than the value of the standard X, then it is seen that the access time on the tested PROM 10 is better than the standard access time required by the thumbwheel setting 25, and the "acceptable" display light 24 will turn on.

It should be noted that when the stop flip-flop 23 is activated to stop the test periods, other possibilities of test information may be accommodated other than just access time.

For example, a display unit could be connected to address register 12 to display the actual address used when a non-correspondence (failure) of data occurred between lines K<sub>a</sub> and K<sub>b</sub>.

Similarly, Exclusive OR gates could be connected between each corresponding information-bit line of K<sub>a</sub> with that of K<sub>b</sub> so that a display unit would indicate exactly "which bits" of memory-output-data have failed to correspond in equality. Thus, many possibilities of gathering test data are available.

The apparatus described herein provides an unexpensive yet fast (1 second or less) system for establishing the reliable access time period for an IC memory such as a PROM.

It should be indicated that other type tests are readily applicable. For example, in FIG. 1, the memory 10 can be subjected to temperature while being exercised. Thus, its operational capability under temperature variations may be analyzed. Likewise, test of memory 10 can be executed while predictably varying the base voltage applied to it, thus also analyzing its behavior under those conditions.

There has been described herein an automatic apparatus for the testing of access time in an integrated circuit memory by which a relatively untrained operator can plug in the memory to be tested, press an initiation button and read out whether the memory is acceptable or rejectable according to a standard set by a thumbwheel time setter. Further, by use of an access time unit, the access time period of the reliability for the memory can be established and identified. The technique and apparatus accomplishes this with merely a few hundred dollars of equipment and in less than one second of time per test compared to the automated test equipment of prior days which required hundreds of thousands of dollars and hours of test time to test a single memory device.

It should be understood that the technique and circuitry described here may be effectuated and accomplished with other equivalent forms of circuitry and devices and it should be understood that the invention is not limited to the specific apparatus involved, but rather is to be defined by the scope of the following claims.

What is claimed is:

1. A test pattern generator system for generating a series of address signals for testing access time of data bits residing in a ROM memory having row and column drivers, said pattern generator system comprising:

(a) counter means providing output signals which increment at a rate established by a second clock means;

(b) clocking means for clocking said counter means, an exclusive OR gate means, and a controlled-delay circuit means, said clocking means including:

(b1) first master clock means for clocking said second clock means at one-half the frequency rate of said first master clock means, and wherein said first master clock means initiates variable-timed test cycles via a controlled delay circuit means to subsequently permit the comparison of first ROM data bits accessed at the start of said test cycle with ROM second data bits accessed at the end of said test cycle;

(b2) said second clock means for clocking said counter means and said exclusive OR gate means;

(c) exclusive OR gate means including a plurality of exclusive OR gates wherein each of said plurality of exclusive OR gates has a first input from said counter means and a second input from said second clock means, and each of said plurality of exclusive

- OR gates provides an output line signal to form a bus means connected to an address register;
- (d) said bus means having a plurality of  $n$  lines, each line functioning to provide one bit of an address signal consisting of  $n$  bits, said bus means connected to an address register of  $n$  bits and providing a  $n$ -bit address signal for temporary storage in said address register;
- (e) said address register for temporary storing address data for subsequent addressing of said ROM memory during said variable timed test cycles;
- (f) an address clock, initiated by said master clock means through said controlled delay circuit means, for clocking address data onto said bus means;
- (g) said controlled delay circuit means for establishing a test cycle of decrementing time periods whereby said delay circuit means releases said ROM second data bits at the end of said test cycle for subsequent comparison.
2. The pattern generator system of claim 1, wherein said bus means is used to convey a series of output addresses to said ROM memory whereby said series of addresses will exercise all combinations of the row and column drivers for each test cycle in a series of test cycles.
3. The pattern generator system of claim 1, wherein said bus means transfers a series of addresses in an increment-complement pattern as a-b-c-d-e-etc. whereby
- a is the initial address
  - b is the complement of a
  - c is the next increment of a
  - d is the complement of c
  - e is the next increment of c, and
- said series of addresses being generated for delivery to said address register means and being usable to exercise each row driver and column driver of said ROM memory.
4. The pattern generator of claim 1, wherein said second clock means includes:
- (i) a divide-by-two flip-flop having an input from said first master clock and providing output clock signals to said counter means and to each exclusive OR gate.
5. The pattern generator of claim 1, wherein said first master clock operates at a one megacycle (megahertz) frequency rate.
- 6.
- In a system for generating address signals for a ROM memory to be exercised, test pattern generation means comprising:
- (a) multiple stage counter means, wherein each stage provides four output signal lines, each of said output signal lines connects to an input of an exclusive OR gate, said multiple stage counter means being clocked by an output signal of a second clock means;
  - (b) first master clock means for toggling said second clock means and for initiating variable-timed test cycles via a controlled-delay circuit means which clocks an address register means;
  - (c) said second clock means having said output signal connected to said counter means and providing an input signal to each of a plurality of exclusive OR gates, said second clock means being used for clocking said OR gate means, wherein said second clock means operates at one-half the frequency rate of said first master clock means;

- (d) circuit means including said exclusive OR gates, each of said OR gates having a first input signal from said counter means and a second input signal from said second clock means, and each OR gate provides an output signal line for carrying one bit of address data via an address bus means;
  - (e) address bus means formed of a plurality of said OR gate output signal lines and functioning to simultaneously carry a concurrent set of address bits for temporary storage in said address register means;
  - (f) said address register means for temporarily storing address data which is clocked to the address lines of said ROM memory at the rate of said first master clock means by an address register clock connected to trigger said address register means;
  - (g) said controlled-delay circuit means, activated by said first master clock, for triggering an address register clock to clock address data from said address register means to said ROM memory;
  - (h) said address register clock connected to said address register means, said address register clock operating to trigger said address register means at the same clock rate of said first master clock means.
7. The pattern generation means of claim 6, wherein said first master clock operates at a 1 megacycle frequency rate.
8. The generation means of claim 6, wherein said address bus means sequentially conveys addresses, whereby the even-numbered sets of addresses are the complement of the preceding odd sets of addresses, and the odd-numbered sequential sets of addresses are incremented over the preceding odd-numbered sets of addresses.
9. The generation means of claim 6, wherein said address bus means sequentially conveys a pattern of addresses to an address register means, whereby said addresses may be sequentially applied to said ROM memory to exercise all the combinations of data in each row and column of said ROM memory.
10. A test pattern generator system for generating a series of addresses for testing access time reliability of data bits residing in a ROM memory having row and column drivers, said pattern generator system comprising:
- (a) address generating means for generating a series of addresses wherein said first, third, and subsequently generated odd-sequences of addresses are incremented by "one", and said second, fourth, and subsequently generated even-sequences of addresses are the complement of the address just preceding, said sequence of address being conveyed to an address register means and functioning to exercise all the row-column combinations of said ROM memory undergoing test during a series of variable-time test cycles;
  - (b) said address register means for temporarily storing each address generated by said address generating means and for subsequently transferring each of said generated addresses to said ROM memory at the frequency rate of a first master clock;
  - (c) address clocking means, connected to said address register means, for triggering the transfer of said stored address in said address register means, to said ROM memory under test, said address clocking means triggering said address register means at the frequency rate of said first master clock;
  - (d) said first master clock for initiating a controlled delay circuit means to periodically activate said

15

address clocking means and also to trigger a flip-flop means which activates said address-generating means at one half the frequency of said first master clock means;

- (e) a second clock which includes said flip-flop means triggered by said first master clock means for activating said address generating means at one-half the frequency rate of said first master clock;
- (f) said controlled-delay circuit means functioning to execute a test cycle during each master clock time-period, whereby said address clocking means initi-

16

ates the application of an address, from said address register means, to said ROM memory under test.

11. The pattern generator system of claim 10, wherein said address generating means includes:

- 5 (a) counter means which provides a plurality of output signals, each signal of which connects as a first input to an exclusive OR gate, said counter means being clocked by said second clock;
- 10 (b) exclusive OR gate means, including a plurality of exclusive OR gates, wherein each OR gate has a second input from said second clock, and each OR gate provides an output line to form an address bus to said address register means.

\* \* \* \* \*

15

20

25

30

35

40

45

50

55

60

65

UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 4,429,389

DATED : January 31, 1984

INVENTOR(S) : Robert D. Catiller

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Col. 11, line 12, change "22b" to --22<sub>b</sub>--.

Col. 11, line 38, change "22b" to --22<sub>b</sub>--.

Col. 11, line 45, change "22b" to --22<sub>b</sub>--.

Col. 12, line 13, between "temperature" and "while",  
insert --variations--.

Col. 14, line 24, change "patern" to --pattern--.

Col. 14, line 51, change "address" to --addresses--.

**Signed and Sealed this**

*Twenty-fourth* **Day of** *April* 1984

[SEAL]

*Attest:*

**GERALD J. MOSSINGHOFF**

*Attesting Officer*

*Commissioner of Patents and Trademarks*